Sigma Delta ADC Virtual Peripheral

Application Note 2

November 2000

1.0 Preface

SX, with its up to 100 MIPS performance , allows efficient implementation of a Sigma Delta converter as a software module (Virtual Peripheral™). The enhanced throughput combined with deterministic interrupt response provides high-speed sampling of an input signal. Sigma delta functions such as modulator, digital filter, and decimator can all be implemented as part of a jitter free interrupt routine with minimal external hardware overhead.

This document outlines the software needed to do analog to digital conversion (ADC) with the SX communications-controller from Ubicom. It also describes the theory of “Sigma Delta ADC” and its implementation on the SX using the concept of Virtual Peripheral. This software may be used with other Virtual Peripheral modules from Ubicom, and with your own application code.

Most of the information found in this document is based on the application note “Sigma Delta ADC Implementation Using the SX Communications Controller” and “A Virtual Peripheral ADC: Using Bitstream A-to-D Conversion”

2.0 Introduction

The Sigma Delta ADC ($\Sigma\Delta$) benefits from all the usual digital advantages, i.e. higher reliability, higher stability and increased functionality. In addition, as sigma delta converter uses mainly digital techniques, it is possible for it to be implemented as a software function in a high performance communications controller.

Successive approximation, dual slope, and flash analog-to-digital converters are all based on the principle of sampling at around the Nyquist frequency and require a good anti-aliasing filter. Sigma Delta ADC, on the other hand, use a low resolution ADC (one bit quantizer) with a sampling rate many times higher than the Nyquist frequency. To implement the sigma delta ADC function as a software module (Virtual Peripheral™) on an microcontroller, the device must offer sufficient processing power to accomplish the high sampling rate.

This application note demonstrates how the SX communications controller can be used to implement an 8-bit sigma delta ADC. Theoretically, the concept can be expanded to achieve even higher resolution by increasing the oversampling rate and using more involved external support circuitry. The paper reviews the theory of operation for a sigma delta ADC, explores techniques to simplify the concept, and adapt the concept to a microcontroller environment.

3.0 Theory of Sigma Delta ADC

A sigma-delta converter consists of a sigma-delta modulator that is essentially a high speed, low resolution ADC, and a digital signal processing stage that trades time for resolution and filters the output of the modulator. The modulator stage samples the analog signal at a large oversampling rate. In this stage, the difference between the input and the output signals is generated and integrated within one or more feedback loops. The output of the integrator is routed through a one-bit quantizer. At efficiently high oversampling rate, the signal change between successive samples is so small that a simple binary quantizer (1 bit converter) can be used. The Nyquist rate is the minimum rate, f_n, at which a quantizer must sample the analog input (bandwidth f_b) to prevent aliasing. The Nyquist rate is equal to twice the bandwidth of the analog input ($f_n=2xf_b$). When a quantizer samples at frequencies higher than the Nyquist rate ($f_s>>f_n$), the digitized input can be faithfully converted back into a continuos analog signal. The sigma-delta converter samples the input signal at many times the Nyquist rate, thus the term “oversampling”.

The output of the quantizer is a pulse density modulated serial bitstream with the high sampling frequency f_s. This serial bitstream, representing the input signal, is passed to a rate reduction, filter (decimation). The decimation stage averages the values and produces n-bit results at lower frequency (Nyquist frequency or higher). A digital filter contained in the decimation stage is to suppress the high frequency noise produced by the quantizer.

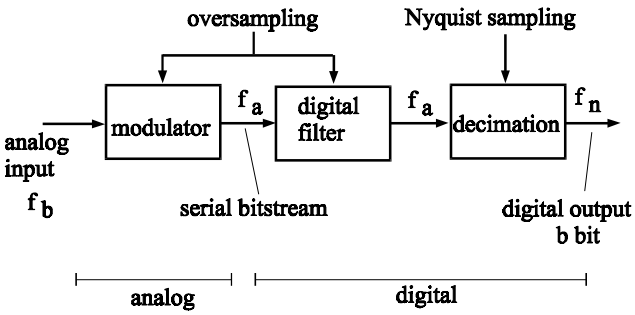

Figure 3-1. Building Blocks of a Sigma Delta Converter

3.1 Modulator

Figure 3-2a shows the block diagram of a sigma delta modulator. The difference (Δ) between the analog input and the comparator's previous output in integrated (∑) in such a manner that the average of the digital output is equal to the analog input. The ones and zeros of a modulator output represent the comparator's positive and negative full scale, respectively. For example, a modulator output of 1, 0, 1, 1, 1, 0, 0, 0, 1, 0, represents an analog input half way between positive and negative full scale (5 ones out of 10 possible values).

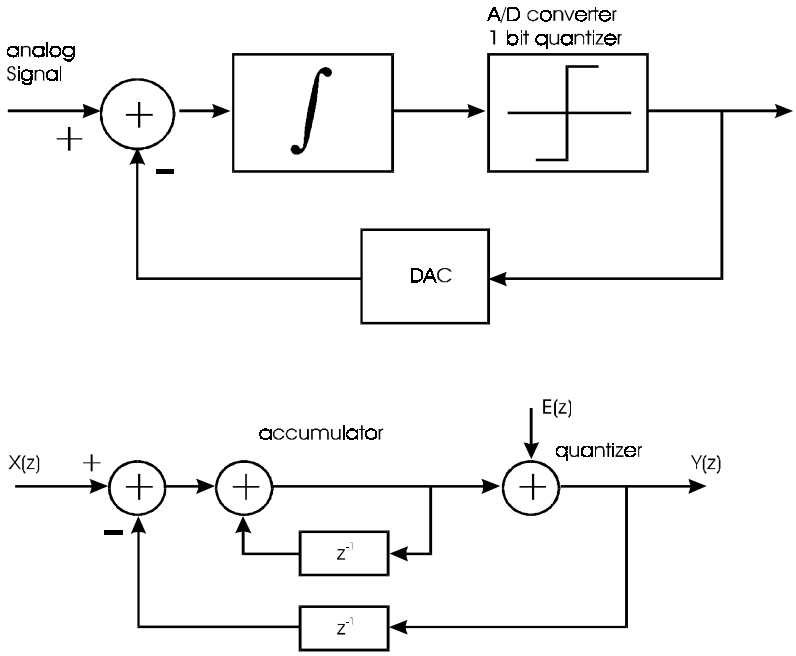

Figure 3-2. Principle of Sigma Delta Modulation a) Building Blocks b) Time Discrete Representation

Output signals are produced at discrete times. The simplest implementation is based on a first order integrator (Figure 3-2b). In Z-domain it represents an accumulator with transfer function:

$$H(z) = \frac{1}{1 - z^{-1}}$$

The quantizer is a non-linear system. For the sake of simplifying the analysis, a linear model of 1- bit ADC is used. Because of the crude approximation made by the comparator of a ∑Δ modulator, a large amount of noise is introduced into the system. This noise can be described as white noise E(z) which is spread out equally over the frequency spectrum. A sine wave input signal power density spectra $S_E(f)$ of the noise depends on the quantization step (Δ).

$$S_E(f) = \frac{1}{f_a} \cdot \frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12 f_a}$$

A quantizer produces white noise only if the following assumptions are met:

- Signal amplitude has to be large relative to the quantization step Δ. This means all quantization steps are really used.
- Input signal is always active, which means all quantization steps are gone through very often.
- Quantization error "e" is moving between -Δ/2 and +Δ/2. Then all values occur with the same probability and quantization error and seem independent of the input signal.

For low frequency signals ($f_b << f_s$), these assumptions are not met, because the real system properties are poorer than what the linear theory predicts. However, the linear model is still an effective tool that can be used to calculate modulator parameters and estimate performance limits.

The feedback loop of the modulator output signal contains a delay of one clock period. In Z-domain the modulator output signal (Figure 3-2b) can be described as:

$$Y(z)=\frac{H(z)}{1+z^{-1}H(z)}X(z)+\frac{1}{1+z^{-1}H(z)}E(z)=X(z)+\left(1-z^{-1}\right)E(z)$$

The input signal X(z) is transmitted to the output with a signal transfer function W(z) = 1 (all pass filter). There is no deformation of the signal spectrum. The quantization noise E(z) is transmitted to the output with noise transfer function $N(z) = 1-z^{-1}$.

In the frequency domain, it is represented as a first order high pass filter (HP1) with characteristics shown in Figure 3-3. Shown also is the noise shaping effect being enhanced by increasing the order of a $\Sigma\Delta$ modulator (adding more integrators). The quantization noise contained in the output signal acquires strong frequency dependence. Due to large oversampling, a greater portion of the noise is shifted to frequencies much higher than the signal bandwidth f_b, which can be filtered through a high pass filter, while the input signal is passed unattenuated at low frequencies. The high-pass function shifts the quantization noise out of the baseband.

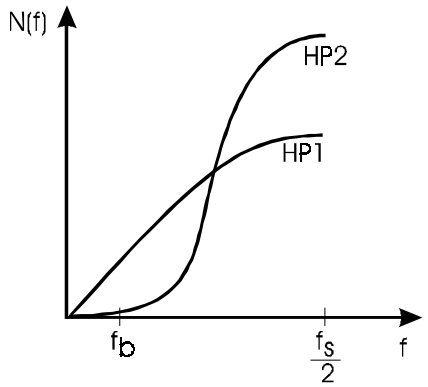

Figure 3-3. Noise Transfer Function

Figure 3-4 shows the timing behavior of integrator output and the binary output of a first order modulator with oversampling rate of 64. The integrator's output oscillates around the comparator's threshold value. Direction and gradient of the integrator output signal is determined by the difference between the analog input and the output of the 1-bit DAC contained in the feedback loop. The digital out changes when the integrator output crosses the comparator's threshold value, causing change to the integration direction. The analog value of the output signal represents the input voltage in the range (U_{Imax} to U_{Imin}). The larger the input voltage, the more "1" values come out of the converter. At low input voltages, "0" values dominate. If the input voltage is at the center, the output value is changed from a 0 to 1 or 1 to 0, depending on what the initial value is. Due to the integrating nature of the modulator, the average value of the output bit stream corresponds to input voltage. Consistency and precision of ADC output, effects the absolute precision of the created average value.

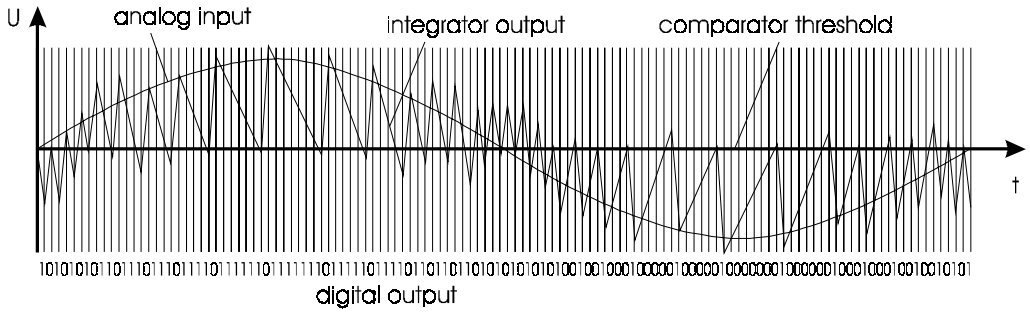

Figure 3-4. Signals in a First Order Sigma Delta Modulator

The signal to noise ratio SNR of the modulator output signal improves with increase in modulator order and the oversampling rate (OSR).

$$SNR_{\max} = 10\lg\left(\frac{3(2n+1)}{2\pi^{2n}}\right)dB + (2n+1)\cdot 10\lg(OSR)dB$$

To analyze the signal to noise ratio, the ratio is compared with the value obtained from an ideal ADC. This value is also called the dynamic range (DR) of a signal. It is calculated as the logarithmic difference between a signal with largest and smallest digital signal value. Signal power of a sine wave signal with amplitude A = $2^{b-1}\,\Delta$, where Δ is quantization step, is:

$$P_S = \frac{A^2}{2} = \frac{\left(2^{b-1}\Delta\right)^2}{2}$$

Noise power of an equally distributed random signal like white noise can be expressed as:

$$P_R = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12}$$

Signal to noise ratio is:

$$DB = SNR_{\max} = 10\cdot\log\left(\frac{P_S}{P_R}\right) = b\cdot 6{,}02\ \text{dB} + 1{,}76\ \text{dB}$$

The relationship is shown in Figure 3-5.

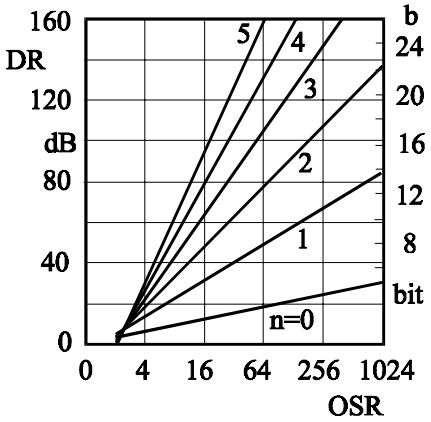

Figure 3-5. Dynamic Range of a Sigma Delta Modulator

As shown in Figure 3-5, to implement an 8- bit ADC with first order modulator, an oversampling rate of 64 is required.

3.2 Digital Filter

The digital part of a sigma delta converter consists of a low pass filter to suppress high frequencies quantization noise and a decimator to reduce sampling frequency of the output signal up to twice the bandwidth of the input signal. The decimation factor "m" must be smaller or equal to the oversampling rate (m ≤ OSR). In simplest way, the low pass filter can be used to generate a moving average of the modulator output.

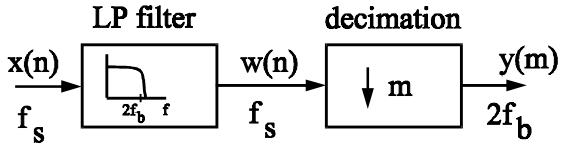

Figure 3-6. Digital Portion of a Sigma Delta Converter

One of the hardest concepts of sigma-delta converters to grasp is how a one bit modulator output is converted into an 8, 12, etc., output words. To achieve resolutions of greater than one bit, the modulator must be decimated. Through decimation, time may be traded for increased resolution. In the decimation process, the modulator output is grouped into blocks. The ones in each block are summed to an output word (sample) is created. The total length of the block determines the resolution of the sample.

The possible "b" value achieved is limited by noise created in the digital filter and decimator. Noise has to be so small that the least significant bit must represent true information. An order k of a low pass filter must have the value k = n+1 (n is the modulator order) to make signal to noise ratio in digital section not worse than that of the modulator.

3.3 Moving Average Calculation

Transfer function of k-th order moving average over "m" sampling points with decimation factor m, can be described in Z-domain as:

$$H_{Si}(z) = \left[\frac{1}{m} \frac{\left(1 - z^{-m}\right)}{\left(1 - z^{-1}\right)} \right]^{k}$$

At multiples of decimator output frequency $f_D = f_s/m$, this transfer function has zeros. This function is specially effective for suppression of disturbances (Figure 3-7).

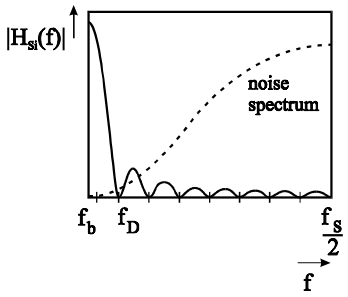

Figure 3-7. Frequency Response of Si-Function

However, the relative flat frequency response is disadvantageous in the initial region of the transfer function $0 < f < f_D$. Only for f_D values much larger then signal bandwidth f_b, the spectral signal influence remains small.

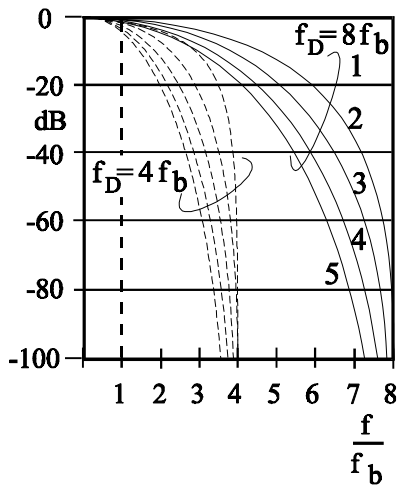

Figure 3-8. Initial Section of Si-Function with Different Orders

With a fourfold decimation, the maximum signal damps of a first order sigma delta ADC amounts to 0.91 dB (Figure 3-8). At $f_D = 8\ f_b$ this value is still 0.22 dB. Problems are also caused by stop-band damping at frequency $f_D - f_b$. This damping is responsible for introducing aliasing into signal band at decimation. In this example, the values are 10.4 dB and 17.08 dB respectively. A moving average of small order is useful only if decimation frequency f_D is much higher than the input signal bandwidth. In all other cases, a much higher order filter must be used. Higher order filters will complicate the filter algorithms and will also limit the sampling frequency.

3.4 ADC Characterization

The ratio between the input voltage and the output sample value (gradient) in a linear ADC should be constant as shown in Figure 3-9 .

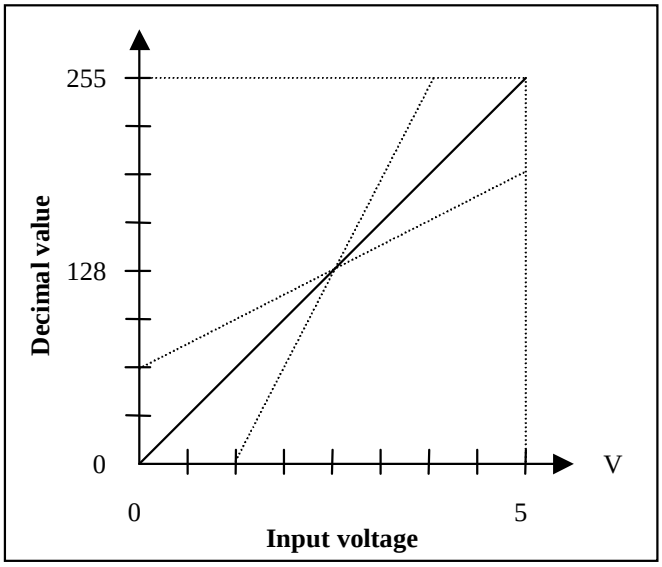

Figure 3-9. Continuous Line Shows the Ideal Linear ADC Transfer Characteristic

However, since the input voltage is an analog value whilst the output sample is digital, a quantization error is introduced. The quantization steps for an 8-bit ADC is:

$$\Delta = \frac{V_{in-range}}{Sample_{range}} = \frac{5V}{2^{n} - 1} = \frac{5}{255} = \underline{19{,}61mV}$$

The min/max input voltage should represent the min/max output sample value. Otherwise, either the input voltage range or the output sample range is not utilized. I.e. when the two resistors at the ADC input (Figure 5-2) are not totally equal, and the effect on the characteristic can be seen as the dotted lines in Figure 3-9.

4.0 ADC Virtual Peripheral Implementation

This 8-bit ADC Virtual Peripheral (`8bitadc.src`) is implemented according to `vp_guide_1.02.src`. The high performance SX allows a simple and cost effective implementation of an 8-bit Sigma Delta ADC with an input range of 0-5V and a minimum of hardware overhead. Applications that do not demand high resolution and speed, such as different kinds of sensors, can use this Virtual Peripheral implementation. Minor modifications of hardware and software are required to accomplish higher resolution and higher accuracy.

4.1 Sigma Delta Modulator

The SX implementation uses a first order modulator. Figure 4-1 shows the circuit diagram based on using an external op-amp as the integrator. The 1-bit quantizer is simply using an input pin configured for CMOS input level. The 1-bit modulator is implemented in software and uses a single output pin. The precision of the ADC is mainly determined by:

- Resistors at the integrator input
- Quality of the on board supply voltage and board design
- Precision of the modulator output pin
- Threshold voltage on the quantizer input pin
- Sampling frequency

The frequency of the input signal is small relative to the sampling frequency. Thus, a sample and hold stage at the converter input is not necessary. An impedance converter (voltage follower) reduces the load presented on the input signal. In addition, if the impedance converter is not present, the internal impedance of the input signal influences the transfer characteristic of the converter (gain). This internal impedance must be added to input impedance of the converter.

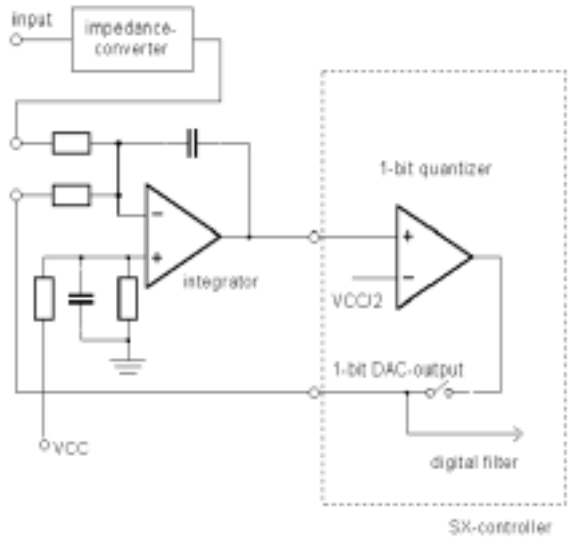

Figure 4-1. Implementation of a First Order Sigma Delta Modulator with Operational Amplifier

If non-linearity at the edges of the measurement can be tolerated, the integrator can be replaced by a simple RC combination as shown in Figure 4-2.

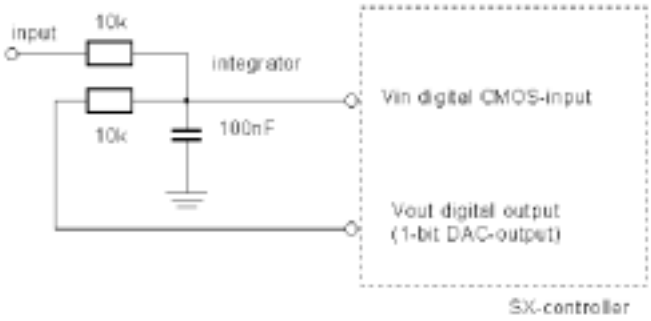

Figure 4-2. Simple Implementation of a First Order Sigma Delta-Modulator

4.2 Virtual Peripheral Description

The circuit is a simple resistor capacitor network connected to two port pins. The implementation uses the SX's internal interrupt feature to allow jitter free background operation of the code as a thread in a Virtual Peripheral.

Essentially, the program code calculates the charge vs. discharge rates of the capacitor according to the voltage applied to the corresponding ADC input. The input triggers when the voltage at the capacitor is crossing ½ V_{DD} (the port pin input and output are set CMOS levels).

One pin is used to monitor the capacitor level, and another one to charge and discharge the capacitor to keep it hovering at the input trigger level. The output is essentially acting like an auto-calibrating pulse width modulator that keeps the capacitor level at $0.5V_{DD}$ using real-time feedback to the input pin. The charge-/discharge times depends on the voltage being applied to the corresponding ADC input. By measuring the charge time vs. (charge + discharge) time ratio, the voltage presented at the ADC input is determined.

Using *adc0* as our example, the ADC routine increments the *adc0Acc* register each time the ADC input is triggered high. *adc0Count* is incremented in each pass through the tread. A sample is taken as soon as *adc0Count* rolls over from 255 to 0, whereupon the value contained in *adc0Acc* is copied to *adc0.* After 256 samples, *adc0Acc* is cleared and a new converting cycle is started. The voltage level on the input pin is proportional to the value in *adc0*:

$$adc0 \,/\, \mathrm{OSR} = V_{adc0\text{-}input} \,/\, V_{DD};\ \mathrm{OSR}=256\ t$$

A value of 00h represents 0V, and a value of FFh represents 5V.

Figure 4-3 shows a flowchart of the algorithm. The 1-bit quantizer and the digital filter are served in a jitter free interrupt routine.

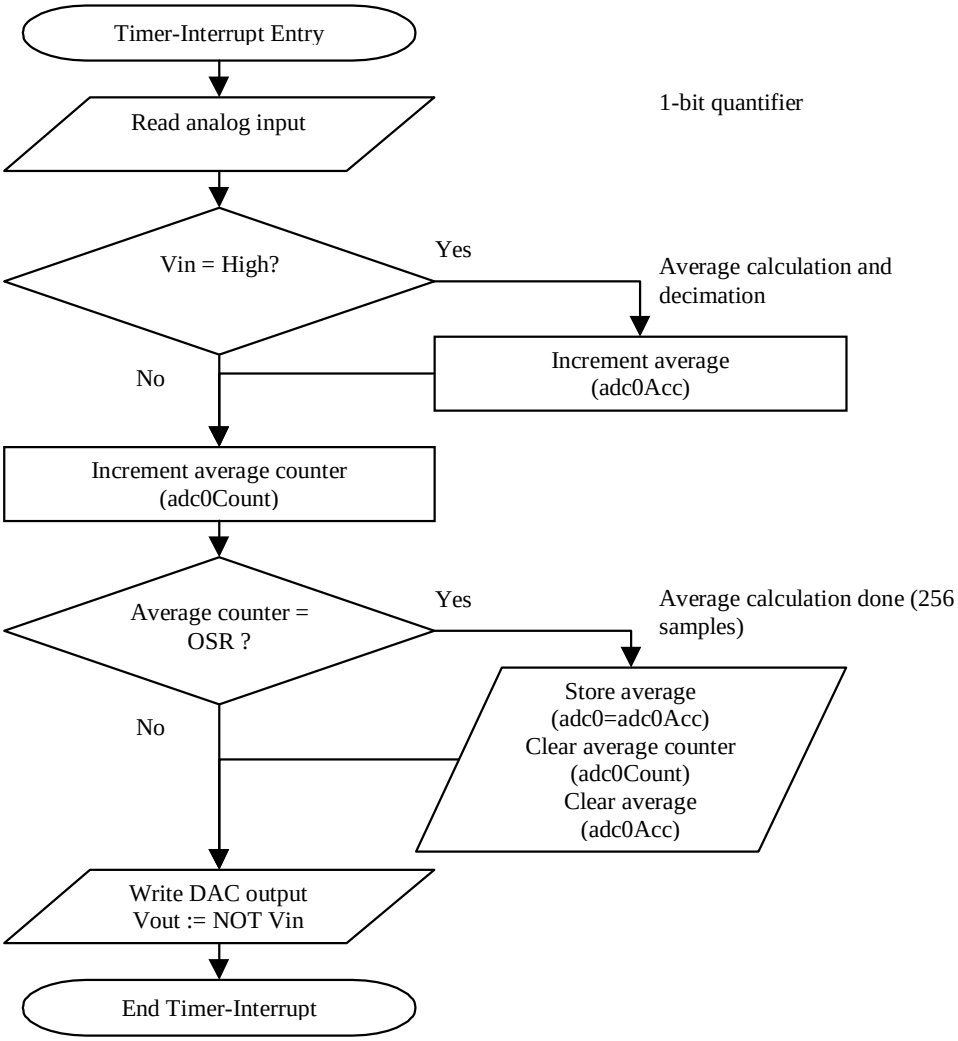

Figure 4-3. Software Routine

4.3 Definition of Parameters

To implement an 8-bit Sigma Delta ADC, an oversampling rate of 64 or more is necessary (Figure 3-5), but since a simplified linear model is used, higher over-sampling rates will provide more accurate results. An oversampling rate (OSR) of 2^8 (256) can be easily achieved with an appropriate software routine. Oversampling rates smaller than 2^8 require lower sampling frequencies, but the software routine demands a larger portion of the CPU time.

Theoretically, it is possible to increase the resolution of ADC by increasing the oversampling rate (e.g. 12 or 16 bit). In addition, higher orders of the modulator and digital filter may be required as well. Increased resolution will also decrease the useful signal bandwidth. To minimize the computation time of the digital filter, only a first order filter was used. Higher order filter need to be used if signal to noise ratio (Figure 3-6) and distortion of measured values at high signal frequencies (Figure 3-8) are not acceptable.

The interrupt rate can be found:

$$InterruptRate = \frac{f_{osc}}{InterruptPeriod \cdot prescaler}[Hz]$$

From this formula we can derive the sample frequency:

$$f_{S,ADC} = \frac{InterruptRate \cdot ThreadRate}{OSR}[Hz]$$

Where:

fosc: Oscillator frequency on the SX.

InterruptPeriod: The number of RTCC cycles between each timer interrupt (*int_period*)

InterruptRate: Interrupt frequency.

ThreadRate: How often, relative to the *InterruptRate*, this Virtual Peripheral runs.

Due to Nyquist's theorem, useful information can only be obtained for frequencies ≤ half of the sample.

$$f_{b,max} = f_{S,ADC} / 2$$

In practice, even signals at or near this frequency will not sample with 8 bits of resolution.

For this the default settings in the *"8bitadc.src"* implementation, we can calculate $f_{b,max}$:

$$InterruptRate = \frac{50MHz}{217 \cdot 1} = \underline{230,4kHz}$$

$$f_{S,ADC} = \frac{230,4kHz \cdot 1/4}{256} = \underline{225,0Hz}$$

By this we can see that the ADC will be able to monitor signals at or below:

$$f_{b,max} = 225,0 / 2 = \underline{112,5Hz}$$

At frequencies above this, the ADC will begin to provide inaccurate information. By increasing the *InterruptRate* and/or the *ThreadRate,* higher frequencies can be monitored. However, increasing the sample frequency ($f_{S,ADC}$) beyond the range of the LP-filter (RC-network) will cause an increasing current drain from the input source.

4.4 Important Considerations

The location of the input and the output pins are hard coded. The input pin has to be located next to the output pin, because the port is read, shifted right, inverted and written out again. If you want to move the pins freely (separate them) by changing the code, some processor power will be lost. Another consideration is that all the port pins are changed in this operation. These remaining pins can be used as additional ADC pins with only simple modifications to the code (replication inside the ADC thread).

The resolution of the Sigma Delta ADC is proportional to the oversampling rate (OSR), but due to circuit noise, the last few bits (+1 or 2 LSB's) should usually be thrown away.

The simple resistor/capacitor combination (Figure 4-2) causes a current drain from the input source in order to maintain the calibration at ½ V_{DD}. The effect of this is equivalent to having the input source connected to 2.5 volts. Thus, current drain considerations on the input source should be kept in mind.

Since timing is critical for accurate readings, make sure that any code executed in the interrupt prior to the ADC code section maintains a uniform execution rate at all times. Remedy this by placing it before any varying execution rate and state dependent code (it should always come before the UART for instance). This is not a consideration if the ADC runs in a separate thread.

It should be noted that changing the timing (like the *int_period*, thread rate and clock speed) only influences the sample rate as long as there is enough MIPS available.

4.5 Specifications of the ADC

Operational mode:	Continuous AD converter
Clock speed:	50MHz
MIPS usage:	2.19 MIPS
Max cycles in each thread:	38
Over Sampling Rate:	256
Sample rate:	225Hz
Resolution:	8 bit
Linearity:	±0.4% (0.5V - 4.5V), ±1.6% (0V – 5V)
RAM usage:	3 bytes in bank 1, plus 1 byte global temp variable
Pin usage:	2 pins used, but 1 port is reserved for AD converting.
RTCC setting:	Timer interrupt running every 4.34µs for 230.414kHz speed
Ubicom mnemonics:	Yes
Multithreaded:	Yes
Thread Rate:	1/4

5.0 Test Description

For the user of the Virtual Peripheral this chapter is an overview of the tests performed to do quality assurance (QA) of the Virtual Peripheral's functionality and integration.

5.1 Test Environment

The Sigma Delta ADC Virtual Peripheral was tested on several different pins and ports on the SX 28-52 Demo Board. These tests was done to:

- Minimize noise affecting the values
- Average pin and port differences
- Average/minimize measurement errors

The purpose of the tests was to check for correct operation and to do a wider characterization of the ADC. The equipment used when testing the 8-bit ADC Virtual Peripheral are listed below:

Oscilloscope	:	Tektronix TDS 3034 (300MHz)
Demo board(s)	:	SX 28-52 demo board
SX Key assembler	:	SX 18/28 Key version 1.09 rev E/F
		SX 48/52 Key version 1.19
SASM assembler	:	SASM version 1.44.6.
Debugger	:	Parallax SX Key rev. E
Passive ADC components	:	Resistor: 2 10kOhm 2% metal film
		Capacitor: 100nF and 10pF Ceramic CK0BX
External DC-supply components	:	2.2kOhm pot. meter
		220Ohm pot. meter
		100nF Ceramic CK0BX 10%

To simulate an adjustable DC voltage supply, a 2,2k variable resistor was used to adjust the voltage from 0-V_{DD}. However, a 220ohm variable resistor was added for fine adjustments (see Figure 5-1).

Ripple voltage noise on the V_{DD} and output pin affected the measurements. Most of this ripple voltage noise could be seen as a 50MHz component; the same as the operating frequency of the SX. This is due to the drained current when all the internal transistors toggle (see Appendix A for details). To compensate for the V_{DD} ripple on the "DC out", a capacitor was added on the *DC out* as shown in Figure 5-1.

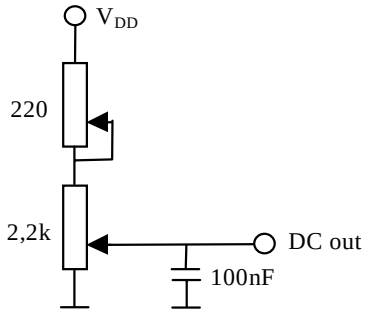

Figure 5-1. DC Voltage Supply

To reduce some of the ripple noise on the output pin, an extra capacitor (10pF) were added in parallel to the existing 100nF (Figure 5-2). The SX ADC Virtual Peripheral was tested in the same environment on all the different pin and port settings, and with the same test setup. The schematic of the test environment is shown in the Figure 5-2.

The *DC out* in Figure 5-1 connected the *Input* in Figure 5-2. However, the passive components in Figure 5-2 were physically located on the same board as the DC voltage source in Figure 5-1. This made it very simple to change between and measure different input and output pins for the ADC, by moving the wires to new input/output pins on the SX. By using the same passive components in all the tests, one possible "error source" was kept constant. The "DC voltage source" was connected to V_{DD} and GND on the SX 28-52 Demo Board.

The oscilloscope was used to measure the input DC voltage, and to view the *Output* signal from the SX ADC. The DC voltage was measured with the *mean* function on the scope.

In addition to this test setup, the *adc0* value was written to port B, which was connected to 8 LEDs. This made it possible to monitor the sampled input in real time and ease the measurements.

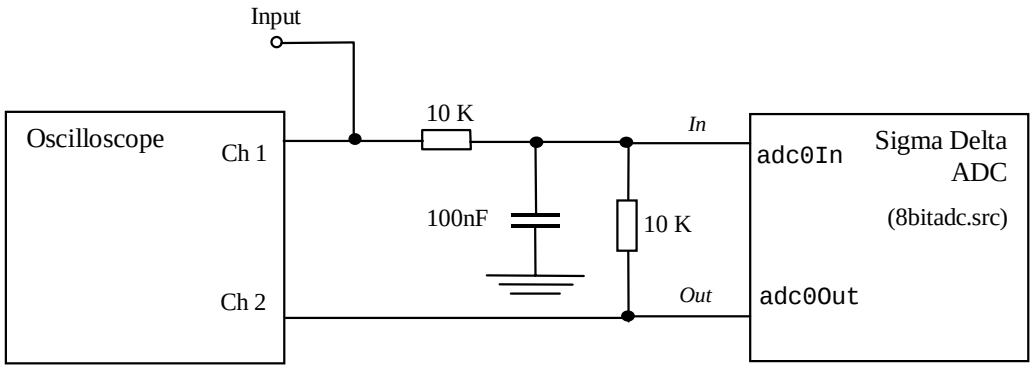

Figure 5-2. Overview of the Test Environment

5.2 Test and Characterization Description

The verification of the Sigma Delta ADC Virtual Peripheral consisted of several tests:

- DC accuracy / linearity
- Deviation with different pin and port configurations
- Over sampling rate

Only the mean results from the tests are shown in section 5. For a complete set of results, see Appendix B.

5.3 DC Measurements

The DC voltage supply was regulated from 0 to 5V, in steps of 0.5V. When the voltage was correctly adjusted, the debugger was "polled" several times. A watch was added in the debugger's window to read the 'digital' output values (see Parallax SX Key/Blitz development system manual on how to use the watch directive).

For some voltage levels, the output value (LSB) in the watch window toggled between two values. So, to be able to establish a reliable result, multiple measurements were done for the same input voltage, and the most frequently read value was registered.

5.3.1 SX28AC

The ports and pins that were tested for the SX28AC:

Table 5-1. Ports and Pins Tested on SX28AC

Port	Input pin	Output pin
A	3	2
A	1	0
C	7	6
C	5	4
C	3	2
C	1	0

Figure 5-3 shows the difference between the expected values (ideal linear ADC) and the actual values for the “Sigma Delta AD Converter”.

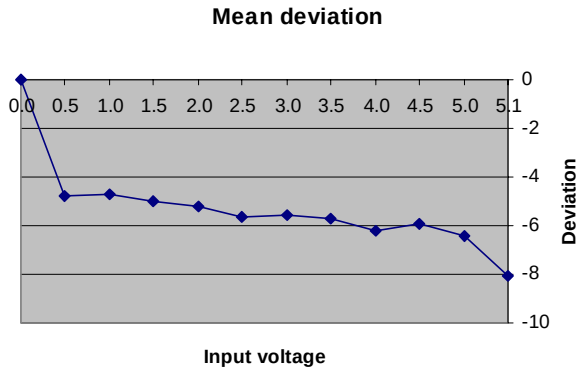

Figure 5-3. ADC Test Result for the SX28AC

Table 5-2. ADC Test Result for the SX28AC

Input	Actual	Expected	Difference
0,00	0,00	0,00	0,00
0,50	20,17	24,93	-4,76
1,00	45,17	49,85	-4,69
1,50	69,75	74,78	-5,03
2,00	94,50	99,71	-5,21
2,50	119,00	124,63	-5,63
3,00	144,00	149,56	-5,56
3,50	168,75	174,49	-5,74
4,00	193,17	199,41	-6,25
4,50	218,42	224,34	-5,92
5,00	242,83	249,27	-6,43
5,12	246,92	255,00	-8,08

As can be seen from the figure above, the output varies from 0 to –8.08 least significant bits.

Figure 5-4 shows the same deviation in percents.

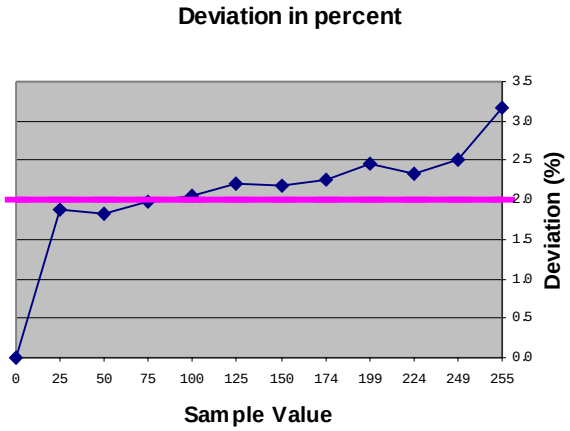

Figure 5-4. Deviation in Percent (SX28AC)

Table 5-3. Deviation in Percent (SX28AC)

Expected	Deviation	Percent (%)
0,00	0,00	0,00
24,93	-4,76	1,87
49,85	-4,69	1,84
74,78	-5,03	1,97
99,71	-5,21	2,04
124,63	-5,63	2,21
149,56	-5,56	2,18
174,49	-5,74	2,25
199,41	-6,25	2,45
224,34	-5,92	2,32
249,27	-6,43	2,52
255,00	-8,08	3,17

5.3.2 SX52BD Device

The ports and pins that were tested for the SX52BD:

Table 5-4. Ports and Pins Tested on SX52BD

Port	Input pin	Output pin
C	1	0
C	3	2
C	5	4
C	7	6
D	1	0
D	3	2
D	5	4
D	7	6
E	1	0
E	3	2
E	5	4
E	7	6

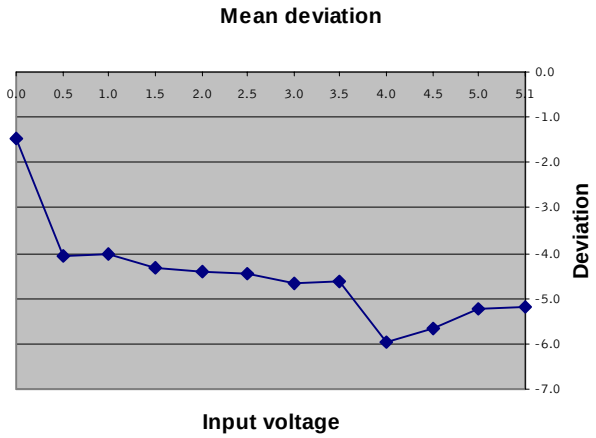

Figure 5-5. ADC Test Result for the SX52BD

Table 5-5. ADC Test Result for the SX52BD

Input	Actual	Expected	Difference
0,03	0,00	1,49	-1,49
0,50	20,75	24,81	-4,06
1,00	45,58	49,61	-4,03
1,50	70,08	74,42	-4,33
2,00	94,83	99,22	-4,39
2,50	119,58	124,03	-4,44
3,00	144,17	148,83	-4,67
3,50	169,00	173,64	-4,64
4,00	192,50	198,44	-5,94
4,50	217,58	223,25	-5,67
5,00	242,83	248,05	-5,22
5,14	249,83	255,00	-5,17

As can be seen from the figure above, the output varies from 0 to –5.94 least significant bits. Figure 5-6 shows the same deviation in percents.

Table 5-6. Difference in Percent (SX52BD)

Expected	Deviation	Percent (%)
1,49	-1,49	0,58
24,81	-4,06	1,59
49,61	-4,03	1,58
74,42	-4,33	1,70
99,22	-4,39	1,72
124,03	-4,44	1,74
148,83	-4,67	1,83
173,64	-4,64	1,82
198,44	-5,94	2,33
223,25	-5,67	2,22
248,05	-5,22	2,05
255,00	-5,17	2,03

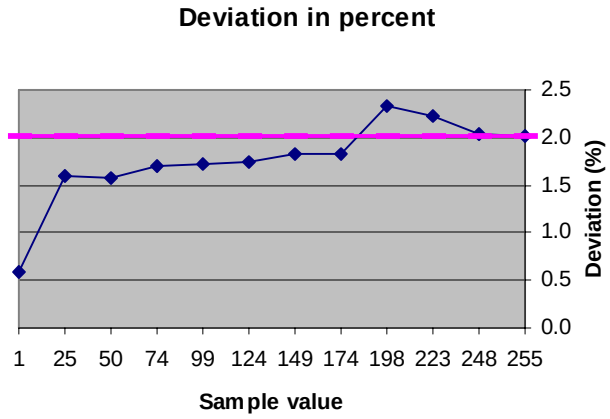

Figure 5-6. Difference in Percent (SX52BD)

5.4 Over Sampling Rate

The sampling frequency can easily be found when the input voltage is adjusted to approx. ½ V_{DD} (where the sampled value is 7Fh/80h). The signal on the *output* pin from the ADC will have a duty cycle of 50%, and the sampling rate is then the twice of the output signal. See Figure 5-7.

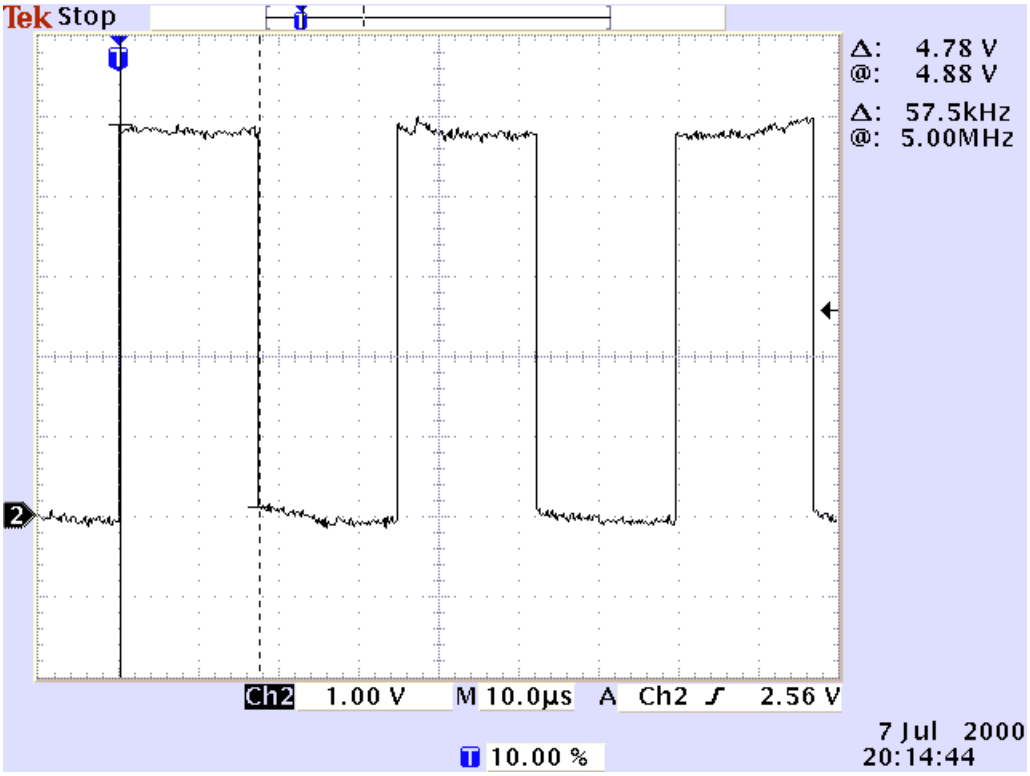

Figure 5-7. Output Signal from ADC at V_{in}= ½ V_{DD}

As can be seen from the figure, the input sampling frequency (for this implementation of the SX ADC) is approximately 57.5kHz. With the current OSR=256, this results in a output sample frequency of:

$$f_s = \frac{f_{s,OSR}}{OSR} = \frac{57.5kHz}{256} = 224.6Hz$$

This is very close to the sample frequency determined in the Virtual Peripheral. The deviation is mainly because of inaccuracy measurement of the $f_{s.OSR}$.

5.5 Conclusion

The measurements indicate that there can be a minor difference between different pins and ports. Even though, the average results shown in Figure 5-6 and Figure 5-5 represents a trend.

- **Negative Mean Deviation**
  All of the individual test results showed that the sampled values was less or equal to the expected ones. An easy way to improve and compensate, is to add an offset value to the `adc0` variable in the code. In our case it would have been appropriate to add a constant in the range 4 to 6. However, the results achieved in this document are not based upon a wide enough study to conclude that this is the absolute correct value. More measurements should be done if more accuracy is needed. **Note!** Care must be taken if the value added causes the adc0 to exceed FFh at 5V input voltage (or 00h at 0V input if the value must be subtracted).
- **Linearity**
  Common for all measurements is that the ADC is acting linear in the range of 0.5V-5V (4.5V). In our case, the ADC is offset but linear with ±0.4% accuracy in the range of 0.5 to 4.5V (based on the mean deviation, see section 6.3).
  The non-linearity in the range 0V-0.5V (and perhaps 4.5V-5V) can be explained from the simple RC-integrator (Figure 4-2). If linearity over the entire input range is required, the ADC should be implemented with an operational amplifier integrator (see Figure 4-1).

This Virtual Peripheral is a simple, but linear and accurate, Sigma Delta ADC under the following circumstances:

1. Offset deviation can be compensated for or disregarded
2. Linear characteristic can be limited to input voltage range 0.5V to 4.5V

5.6 Sources of Error

The first obvious source of inaccuracy is the nature of the measurement:

- Varying the input voltage in steps
- Manually measure the input voltage
- Manually read of the sampled value

Different resistance between the two resistors at the ADC input (shown in Figure 5-2) influences the gradient of the AD characteristic. A difference of only 1% can introduce ±1 LSB error (2% tolerance resistors can theoretically introduce ±5 LSB deviation). Thus, high precision resistors with low tolerance should be used.

The effect the ripple voltage noise on the input signal and the ADC output pin has at the result is very complex to decide. However, ripple noise exceeding the quantization noise will affect the sampled result. Efficient onboard decoupling should be done to reduce the amount of this noise. Another simple solution is to throw away some bits (1 or 2 LSB).

Comparing the results with a “continuous ideal analog” transfer characteristic, introduces the quantization error in the results. The quantization error in the samples (results) is ± 0,5 digits (LSB).

6.0 References

Ref.:	Title	Author	Date
	An Analysis of Nonlinear Behaviour in Delta-Sigma Modulators. (IEEE Trans)	Ardalan, S. H. Paulos, J.J	
	Circuits and Sys (Vol. CAS-34, p. 593-603)		June 1987
	Entwurfskonzept für Sigma-Delta-A/D-Wan-dler. Diplomarbeit, Fak. Elektrotechnik, TU Dresden (Germany)	Becker, S.	1996
	Oversampling Delta-Sigma Data Converters. (IEEE Press)	Candy, J.C. Temes, G.C.	1991
	Decimation for Sigma Delta Modulation. (IEEE Trans. Commun., vol. COM-34, p. 249-258)	Candy, J.C.	Jan. 1986
	Quantization Noise Spectra. Trans. Inform. Theory (Vol. IT-36, p. 1200-1244)	Gray, R.M.	Nov. 1990
	Signalübertragung. (Springer-Verlag)	Lüke, H. D.	1990
	µController mit virtueller Peripherie, (Design&Elektronik, vol. 6/98 p.32-34)	Wurlitzer, Th.	June 1998
	Kompakt-klasse (ELRAD, vol. 2-4/98)	Thamm,O. Wurlitzer, Th. Hertenberger, A.	1998
	Sigma Delta ADC Implementation Using the SX Communications Controller	Wolfgang, R. Wurlitzer, T.	
	A Virtual Peripheral ADC: Using Bitstream A-to-D Conversion		

7.0 Appendix A

This appendix contains information earlier found in the “Sigma Delta ADC Implementation Using the SX Communications Controller” (see section 7).

7.1 Observations

Figure 7-1 and Figure 7-2 show the characteristics of the quantizer input. The threshold voltage is set at half the supply voltage (2.49 V) and has a hysteresis of approx. 2 mV. Undesired oscillation was observed when the threshold voltage was crossed at a very slow rate (milliseconds). This effect appeared only during measurement and was not observed during actual operation.

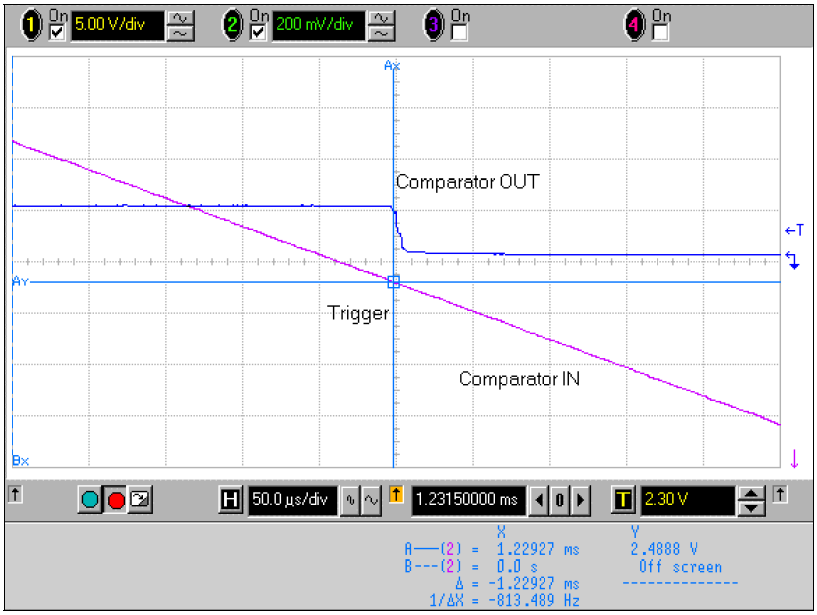

Figure 7-1. Transfer Characteristic of Digital CMOS Input with Linearly Decreasing Input Voltagext

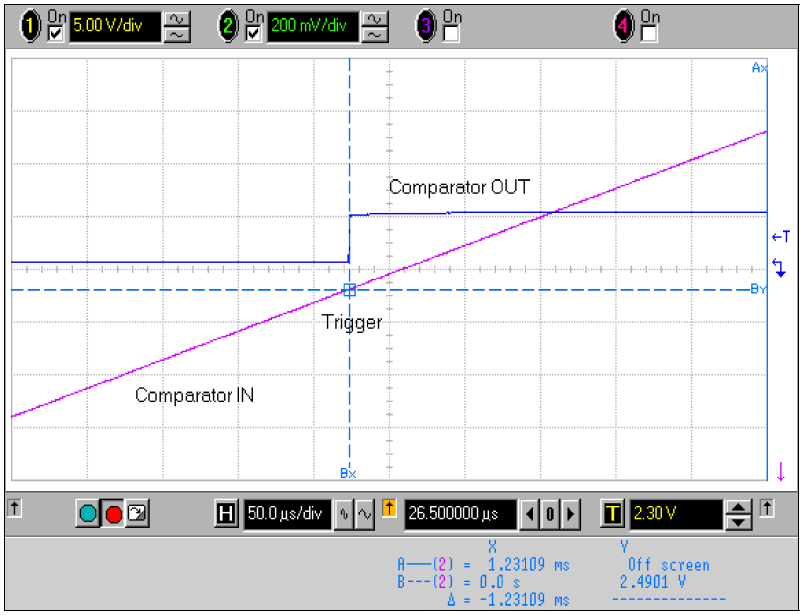

Figure 7-2. Transfer Characteristic of Digital CMOS Inputs with Linearly Increasing Input Voltaget

The precision of comparator and DAC output is influenced by the quality of the reference voltage. This experiment relied directly on the SX supply voltage. A separate reference voltage was not used. Since the SX high operating frequency (50 MHz) generates higher current drain, a fair amount of supply voltage bounce was observed. Figure 7-3 shows peak to peak voltage bounce of amounts 276 mV on the SX V_{dd} pin.

The influence of the supply bounce on system parameters can be partially compensated through fixed phase sampling that corresponds to the bounce. If the precision of the sigma delta modulator does not meet the application requirement, a separate reference voltage may be needed for the DAC output.

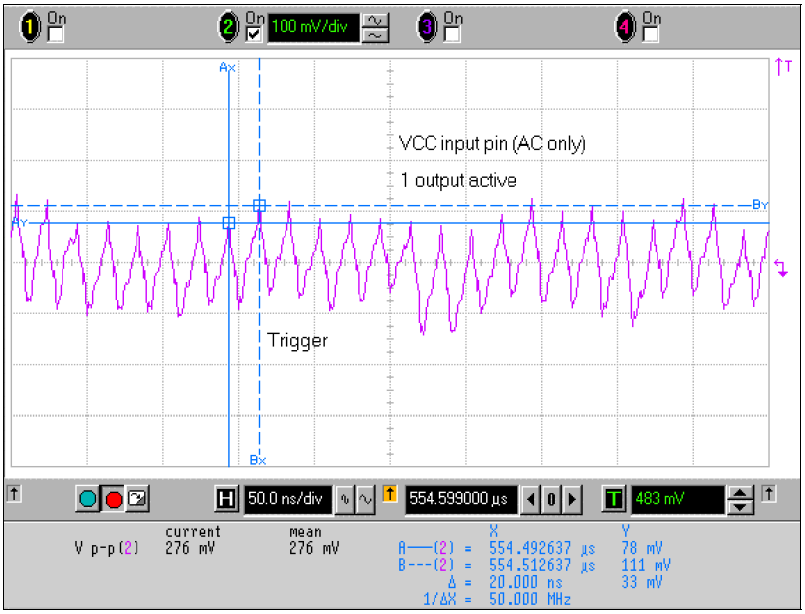

Figure 7-3. Voltage Bounce at V_{DD} Pin

Figure 7-4 shows the output pin voltage at high level. The average value is around 4.84 V with a voltage bounce of 385 mV. This small average value produces a systematic converter gain error.

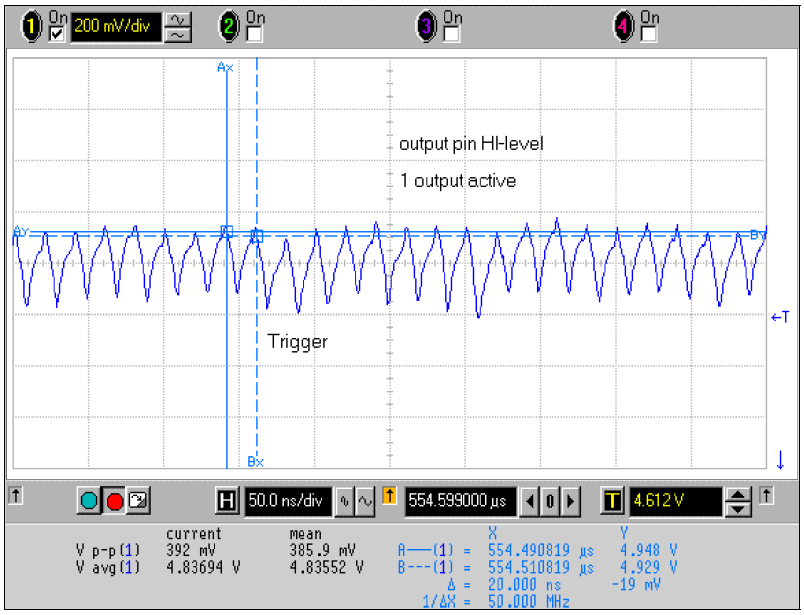

Figure 7-4. Output Voltage at High Level

Figure 7-5 shows the output pin voltage at low level. The voltage bounce level is the same, but the average value is nearly ideal.With the 1-bit DAC output signal present at the integrator input, the integrator output signal looks similar to the signal shown in Figure 7-5 output.

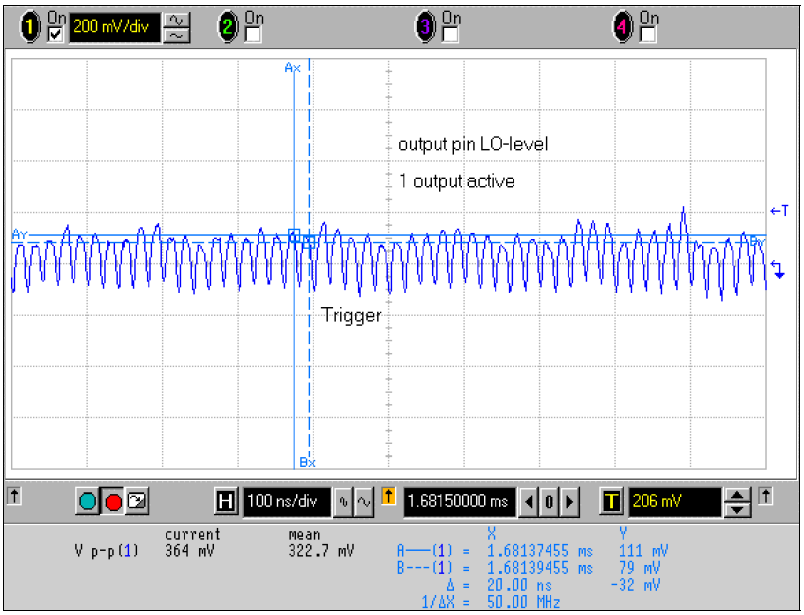

Figure 7-5. Output Voltage Low Level

An illustration of the signal characteristics is shown in Figure 7-6 for a sampling frequency of 30.6 kHz and a constant input voltage of 4 V.

A signal stroke of about 180mV is created at the integrator output containing the bounce shown earlier (the value varies around the threshold of 2.5 V).

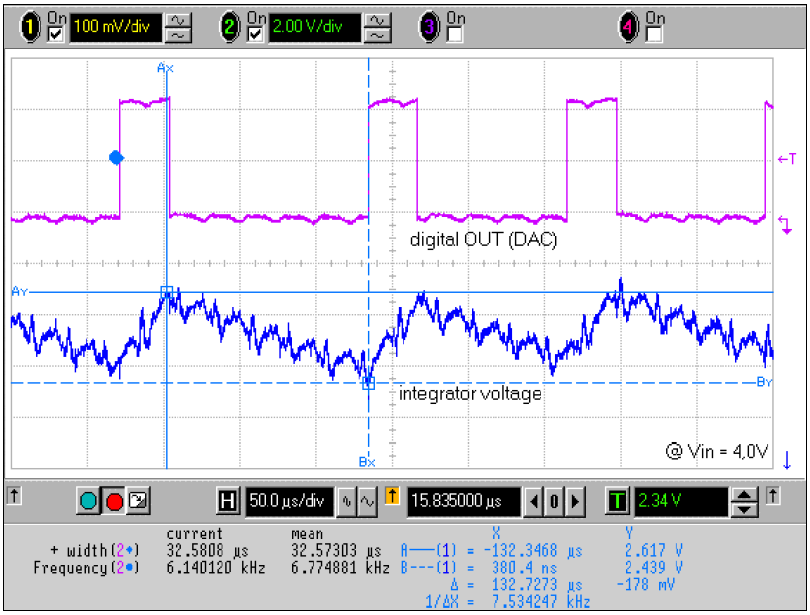

Figure 7-6. Integrator Voltage at 30.6 KHz Sampling Frequency

If the sampling frequency is raised to a realistic value such as 306 KHz, the signal stroke decreases to 20 mV (Figure 7-7). This level is enough to reliably switch the comparator . Sampling points are determined by software and are positioned 140 ns in front of the DAC output switching points. If the signal stroke is adequately small, the integrator behavior can be assumed to be linear.

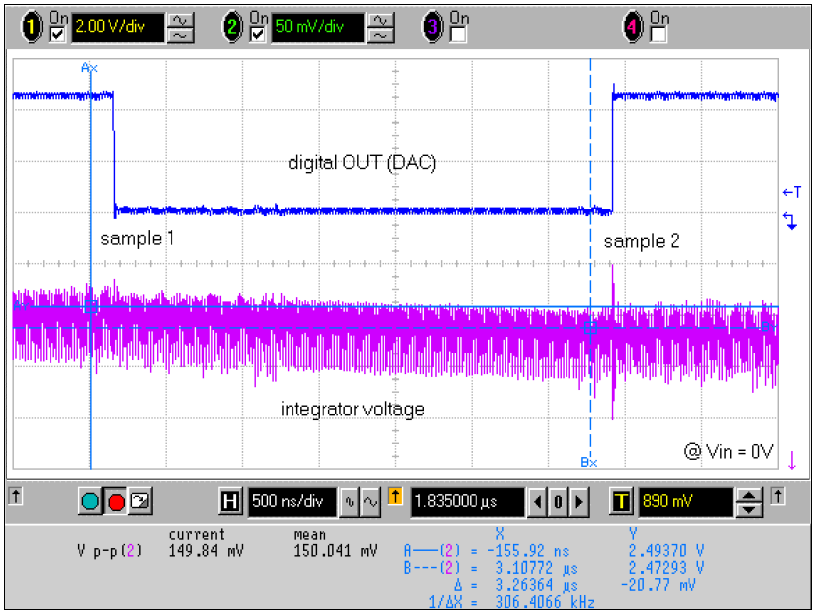

Figure 7-7. Integrator Voltage at 306 KHz Sampling Frequency

7.2 Results

To determine the static transfer characteristic of the ADC, all measurement results are compared with values obtained from an industrial 12-bit ADC. Figure 7-8 shows the absolute error in digits as the input voltage is linearly increased from 0 to 4 V. The difference between input voltage and the measured value is plotted.

The systematic error (slope of error characteristic) is due to following:

- Low precision of the resistors used at the integrator's input
- Influence of the input signal internal impedance that is added to the integrator's input impedance

It is possible to suppress the systematic errors by using an input voltage follower and an external ADC output voltage and by equalizing the input resistances. Then the only disturbance that remains is noise.

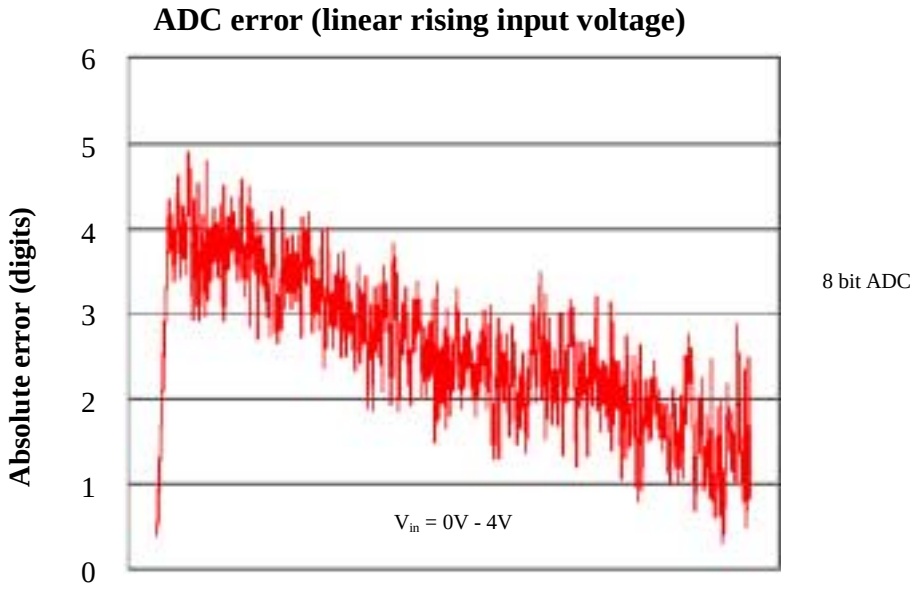

Figure 7-8. Absolute Error of 8 Bit Sigma Delta DAC in Digits (LSB)

Figure 7-9 shows the ADC noise error. The 1 to 2 LSB noise error is present due to the use of a first order modulator and a first order digital filter.

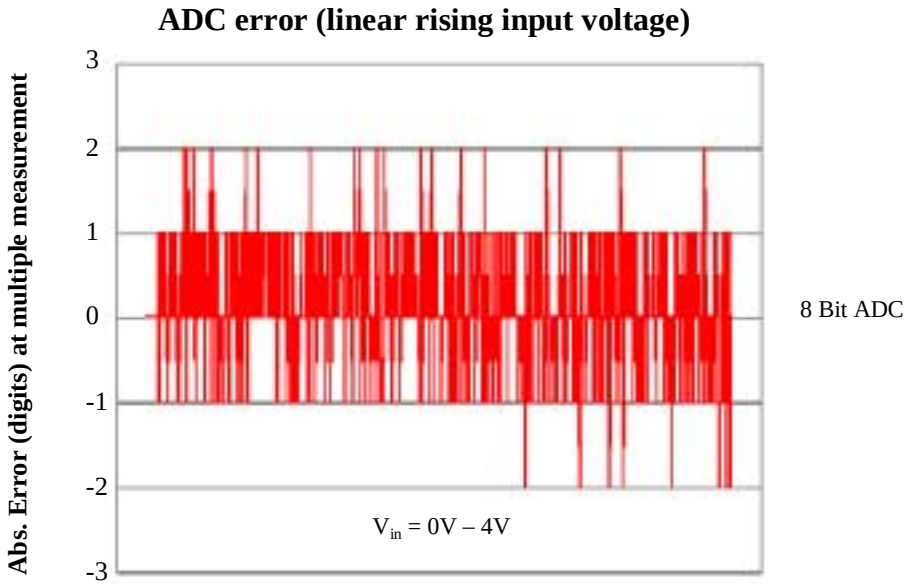

Figure 7-9. Absolute Noise of 8 Bit Sigma Delta DAC in Digits (LSB)

7.3 Conclusions

The high performance SX allows a simple and cost effective implementation of an 8-bit sigma delta ADC. With SX implementation, an accuracy of 2% can be achieved if systematic errors are compensated. Additional modifications of hardware and software are required to accomplish higher resolution and higher accuracy. Applications that do not demand high resolution and speed s (temperature compensation, sensors) can use the approach with its low cost and simple hardware.

8.0 Appendix B

All the tests were performed on SX 28-52 Demo board. This appendix contains a complete overview of the test results for both SX28AC and SX52BD, with different port and pin settings. These results are the foundation for section 6.

8.1 SX28AC Device

On the SX28AC there was performed the same test for the DC accuracy for six different port and pin configuration. The entire test results for the SX28AC are listed in the table below:

Table 8-1. Test Result - SX28AC

Port A pin 3 and 2		Mid value:	2,69 V
Input	**Actual**	**Expected**	**Difference**
0,00	0	0,00	0,00
0,50	21	24,81	-3,81
1,00	46	49,61	-3,61
1,50	70	74,42	-4,42
2,00	95	99,22	-4,22
2,50	119	124,03	-5,03
3,00	144	148,83	-4,83
3,50	168	173,64	-5,64
4,00	193	198,44	-5,44
4,50	218	223,25	-5,25
5,00	242	248,05	-6,05
5,11	246	253,51	-7,51

Table 8-2. Test Result - SX28AC

Port A pin 1 and 0			
Input	**Actual**	**Expected**	**Difference**
0,00	0	0,00	0,00
0,50	23	24,81	-1,81
1,00	48	49,61	-1,61
1,50	73	74,42	-1,42
2,00	97	99,22	-2,22
2,50	121	124,03	-3,03
3,00	146	148,83	-2,83
3,50	171	173,64	-2,64
4,00	195	198,44	-3,44
4,50	219	223,25	-4,25
5,00	244	248,05	-4,05
5,07	245	251,53	-6,53

Table 8-3. Test Result - SX28AC

Port C pin 7 and 6			
Input	**Actual**	**Expected**	**Difference**
0,00	0	0,00	0,00
0,50	17	24,81	-7,81
1,00	42	49,61	-7,61
1,50	67	74,42	-7,42
2,00	90	99,22	-9,22
2,50	117	124,03	-7,03
3,00	142	148,83	-6,83
3,50	167	173,64	-6,64
4,00	192	198,44	-6,44
4,50	215	223,25	-8,25
5,00	241	248,05	-7,05
5,14	247	255,00	-8,00

Table 8-4. Test Result - SX28AC

Port C pin 5 and 4			
Input	**Actual**	**Expected**	**Difference**
0,00	0	0,00	0,00
0,50	18	24,81	-6,81
1,00	43	49,61	-6,61
1,50	68	74,42	-6,42
2,00	92	99,22	-7,22
2,50	117	124,03	-7,03
3,00	143	148,83	-5,83
3,50	168	173,64	-5,64
4,00	192	198,44	-6,44
4,50	218	223,25	-5,25
5,00	242	248,05	-6,05
5,14	248	255,00	-7,00

Table 8-5. Test Result - SX28AC

Port C pin 3 and 2			
Input	**Actual**	**Expected**	**Difference**
0,00	0	0,00	0,00
0,50	18	24,81	-6,81
1,00	43	49,61	-6,61
1,50	67	74,42	-7,42
2,00	93	99,22	-6,22
2,50	118	124,03	-6,03
3,00	142	148,83	-6,83
3,50	168	173,64	-5,64
4,00	192	198,44	-6,44
4,50	218	223,25	-5,25
5,00	243	248,05	-5,05
5,14	248	255,00	-7,00

Table 8-6. Test Result - SX28AC

Port C pin 1 and 0			
Input	**Actual**	**Expected**	**Difference**
0,00	0	0,00	0,00
0,50	19	24,81	-5,81
1,00	44	49,61	-5,61
1,50	69	74,42	-5,42
2,00	94	99,22	-5,22
2,50	119	124,03	-5,03
3,00	144	148,83	-4,83
3,50	168	173,64	-5,64
4,00	193	198,44	-5,44
4,50	219	223,25	-4,25
5,00	243	248,05	-5,05
5,14	249	255,00	-6,00

8.2 SX52BD part

On the SX52BD there was performed the same test for the DC accuracy for twelve different port and pin configurations. The entire test results for the SX52BD are listed in the table below:

Table 8-7. Test Result - SX52BD

Port C pin 1 and 0			
Input	**Actual**	**Expected**	**Difference**
0,04	0	1,98	-1,98
0,50	21	24,81	-3,81
1,00	46	49,61	-3,61
1,50	71	74,42	-3,42
2,00	95	99,22	-4,22
2,50	120	124,03	-4,03
3,00	145	148,83	-3,83
3,50	168	173,64	-5,64
4,00	192	198,44	-6,44
4,50	217	223,25	-6,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-8. Test Result - SX 52

Port C pin 3 and 2			
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	22	24,81	-2,81
1,00	46	49,61	-3,61
1,50	70	74,42	-4,42
2,00	95	99,22	-4,22
2,50	120	124,03	-4,03
3,00	145	148,83	-3,83
3,50	170	173,64	-3,64
4,00	193	198,44	-5,44
4,50	218	223,25	-5,25
5,00	244	248,05	-4,05
5,14	251	255,00	-4,00

Table 8-9. Test Result - SX52BD

Port C pin 5 and 4			2,67V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	23	24,81	-1,81
1,00	47	49,61	-2,61
1,50	71	74,42	-3,42
2,00	96	99,22	-3,22
2,50	120	124,03	-4,03
3,00	145	148,83	-3,83
3,50	169	173,64	-4,64
4,00	192	198,44	-6,44
4,50	218	223,25	-5,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-10. Test Result - SX52BD

Port C pin 7 and 6			2,67V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	21	24,81	-3,81
1,00	46	49,61	-3,61
1,50	71	74,42	-3,42
2,00	95	99,22	-4,22
2,50	120	124,03	-4,03
3,00	145	148,83	-3,83
3,50	169	173,64	-4,64
4,00	193	198,44	-5,44
4,50	218	223,25	-5,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-11. Test Result - SX52BD

Port D pin 1 and 0			2,67V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	20	24,81	-4,81
1,00	45	49,61	-4,61
1,50	69	74,42	-5,42
2,00	94	99,22	-5,22
2,50	118	124,03	-6,03
3,00	143	148,83	-5,83
3,50	168	173,64	-5,64
4,00	192	198,44	-6,44
4,50	217	223,25	-6,25
5,00	242	248,05	-6,05
5,14	250	255,00	-5,00

Table 8-12. Test Result - SX52BD

Port D pin 3 and 2			2,67V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	21	24,81	-3,81
1,00	45	49,61	-4,61
1,50	70	74,42	-4,42
2,00	95	99,22	-4,22
2,50	119	124,03	-5,03
3,00	144	148,83	-4,83
3,50	169	173,64	-4,64
4,00	192	198,44	-6,44
4,50	218	223,25	-5,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-13. Test Result - SX52BD

Port D pin 5 and 4			2,68V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	20	24,81	-4,81
1,00	45	49,61	-4,61
1,50	70	74,42	-4,42
2,00	94	99,22	-5,22
2,50	119	124,03	-5,03
3,00	143	148,83	-5,83
3,50	169	173,64	-4,64
4,00	193	198,44	-5,44
4,50	218	223,25	-5,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-14. Test Result - SX52BD

Port D pin 7 and 6			2,67V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	21	24,81	-3,81
1,00	46	49,61	-3,61
1,50	70	74,42	-4,42
2,00	95	99,22	-4,22
2,50	121	124,03	-3,03
3,00	145	148,83	-3,83
3,50	169	173,64	-4,64
4,00	193	198,44	-5,44
4,50	217	223,25	-6,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-15. Test Result - SX52BD

Port E pin 1 and 0			
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	21	24,81	-3,81
1,00	45	49,61	-4,61
1,50	70	74,42	-4,42
2,00	95	99,22	-4,22
2,50	120	124,03	-4,03
3,00	144	148,83	-4,83
3,50	170	173,64	-3,64
4,00	194	198,44	-4,44
4,50	218	223,25	-5,25
5,00	244	248,05	-4,05
5,14	249	255,00	-6,00

Table 8-16. Test Result - SX52BD

Port E pin 3 and 2			
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	20	24,81	-4,81
1,00	46	49,61	-3,61
1,50	70	74,42	-4,42
2,00	95	99,22	-4,22
2,50	120	124,03	-4,03
3,00	145	148,83	-3,83
3,50	171	173,64	-2,64
4,00	192	198,44	-6,44
4,50	218	223,25	-5,25
5,00	243	248,05	-5,05
5,14	250	255,00	-5,00

Table 8-17. Test Result - SX52BD

Port E pin 5 and 4			
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	20	24,81	-4,81
1,00	46	49,61	-3,61
1,50	70	74,42	-4,42
2,00	96	99,22	-3,22
2,50	120	124,03	-4,03
3,00	144	148,83	-4,83
3,50	169	173,64	-4,64
4,00	192	198,44	-6,44
4,50	218	223,25	-5,25
5,00	242	248,05	-6,05
5,14	249	255,00	-6,00

Table 8-18. Test Result - SX52BD

Port E pin 7 and 6			2,7V
Input	**Actual**	**Expected**	**Difference**
0,03	0	1,49	-1,49
0,50	19	24,81	-5,81
1,00	44	49,61	-5,61
1,50	69	74,42	-5,42
2,00	93	99,22	-6,22
2,50	118	124,03	-6,03
3,00	142	148,83	-6,83
3,50	167	173,64	-6,64
4,00	192	198,44	-6,44
4,50	216	223,25	-7,25
5,00	241	248,05	-7,05
5,14	249	255,00	-6,00

Lit#: AN02-02

For the latest contact and support information on SX devices, please visit the Ubicom website at www.ubicom.com. The site contains technical literature, local sales contacts, tech support and many other features.

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