

PIC24H Family Reference Manual

Register 21-23: CiCTRL1: ECAN™ CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	—	CSIDL	ABAT	CANCKS	REQOP<2:0>		
bit 15					bit 8		

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>				CANCAP			WIN
bit 7					bit 0		

Legend: C = Writable bit, but only '0' can be written to clear the bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode
- bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted
- bit 11 **CANCKS:** CAN Master Clock Select bit
1 = CAN FCAN clock is Fcy
0 = CAN FCAN clock is FOSC
- bit 10-8 **REQOP<2:0>:** Request Operation mode bits
000 = Set Normal Operation mode
001 = Set Disable mode
010 = Set Loopback mode
011 = Set Listen-Only mode
100 = Set Configuration mode
101 = Reserved
110 = Reserved
111 = Set Listen All Messages mode
- bit 7-5 **OPMODE<2:0>:** Operation mode bits
000 = Module is in Normal Operation mode
001 = Module is in Disable mode
010 = Module is in Loopback mode
011 = Module is in Listen-Only mode
100 = Module is in Configuration mode
101 = Reserved
110 = Reserved
111 = Module is in Listen All Messages mode
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
1 = Enable input capture based on CAN message receive
0 = Disable CAN capture
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **WIN:** SFR Map Window Select bit
1 = Use filter window
0 = Use buffer window

REGISTER 19-1: CICTRL1: ECAN™ CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	→	REQOP<2:0>		
bit 15					bit 8		

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>			—	CANCAP	—	—	WIN
bit 7				bit 0			

Legend:	C = Writable bit, but only '0' can be written to clear the bit	r = Bit is Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12 **ABAT:** Abort All Pending Transmissions bit
 1 = Signal all transmit buffers to abort transmission.
 0 = Module will clear this bit when all transmissions are aborted
- bit 11 **Reserved:** Do not use
- bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
 000 = Set Normal Operation mode
 001 = Set Disable mode
 010 = Set Loopback mode
 011 = Set Listen Only Mode
 100 = Set Configuration mode
 101 = Reserved
 110 = Reserved
 111 = Set Listen All Messages mode
- bit 7-5 **OPMODE<2:0>:** Operation Mode bits
 000 = Module is in Normal Operation mode
 001 = Module is in Disable mode
 010 = Module is in Loopback mode
 011 = Module is in Listen Only mode
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- bit 4 **Unimplemented:** Read as '0'
- bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
 1 = Enable input capture based on CAN message receive
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- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **WIN:** SFR Map Window Select bit
 1 = Use filter window
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